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PUB-NO: JP401028940A
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TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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INVENTOR-INFORMATION:

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INT-CL (IPC): H01L 21/82; H01L 27/08

ABSTRACT:

PURPOSE: To enhance the breakdown strength of a latch-up by a method wherein a low-impedance conductor wiring part is connected to diffusion layers of an N+ type diffusion layer and a P+ type diffusion layer via the sufficient number of contact holes and the diffusion layers are fixed completely at a maximum operating potential and a minimum operating potential.

CONSTITUTION: An N+ type guard ring layer 33 and a P+ type guard ring layer 32 which surround a PMOS transistor 30 and an NMOS transistor 31 completely are installed. In addition, a low-impedance aluminum wiring part 18 is installed on these guard ring layers; this aluminum wiring part 18 is connected to the respective gurad ring layers 32, 33 via a number of contact holes 13 made in an insulating film (an SiO2 film) 17 formed on the surface of a semiconductor substrate 19; the guard ring layers 32, 33 are made to be substantially low impedance; a potential of the individual guard ring layers is fixed completely to a ground or a power-supply potential. By this setup, it is possible to enhance the breakdown strength of a latch-up.